Journal of Interfaces, Thin films, and Low dimensional systems 7 (1) Summer and Autumn (2023) 675-684

Performance Investigation of an Extended Source Germanium Reconfigurable Field Effect Transistor for Advanced CMOS Applications

Scientific research paper

Hamid Reza Heydari, Zahra Ahangari*, Hamed Nematian, Kian Ebrahim Kafoori

Department of Electronics, Yadegar- e- Imam Khomeini (RAH) Shahr-e-Rey Branch, Islamic Azad University, Tehran, Iran.

ARTICLE INFO

Article history:
Received 24 August 2023
Revised 30 September 2023
Accepted 13 October 2023
Available online 28 November 2023

Keywords
Schottky barrier transistor
Thermionic emission
Direct tunneling
Reconfigurable transistor

ABSTRACT

This paper presents a comprehensive investigation into the electrical characteristics of a reconfigurable Schottky barrier transistor that utilizes germanium as the channel material and features an extended source region. The impact of critical design parameters on the device performance is thoroughly assessed. The device is capable of achieving both n-type and p-type operation on a single device by adjusting the appropriate bias for the electrodes without the need for additional physical doping. The proposed device offers a wider tunneling area at the interface of the source and channel region, leading to an improvement in device switching performance and a reduction in the threshold voltage required for the onset of tunneling. The gate work function is a crucial design parameter that should be optimized to minimize the off-state current for both n-type and p-type operation. The findings reveal that the on/off current ratio of 5.26×10^4 and 5.9×10^4 can be attained for n-type and p-type operation, respectively. Furthermore, the analog performance of the device has been examined, and a cut-off frequency of f_T=3GHz has been achieved for n-type and p-type device. These results provide valuable insights into the development of low-power reprogrammable logic circuits.

1 Introduction

Nowadays, the pursuit of technology is directed towards the reduction of the dimensions of conventional Metal Oxide Semiconductor Field Effect Transistor (MOSFET) in order to fulfill the ever-increasing demand for high-speed low-power integrated circuits. However, as the device dimension decreases towards the nanoscale regime, short channel effects emerge and degrade the device performance [1-3]. The fundamental solutions to overcome the enhanced leakage current of the device are to increase the gate controllability over the channel and reduce the channel thickness. Nevertheless, fabrication of heavily doped thin film source/drain regions is challenging, and thin film thickness increases the parasitic resistance. Schottky barrier transistor with metal source/drain regions is deemed as an appropriate option for the physically doped source/drain devices [4-7]. The current mechanism of the Schottky barrier transistor is contingent upon the current mechanism of the Schottky diode which is entirely distinct from the conventional MOSFET.

The reconfigurable field effect transistor (RFET) has emerged as a promising alternative to the conventional MOSFET. With the capability to implement both n-type

*Corresponding author.
Email address: z.ahangari@gmail.com
DOI: 10.22051/jitl.2023.44794.1095

(electron conduction) and p-type (hole conduction) devices on a single transistor, this technology employs Schottky barrier transistors to overcome the need for additional physical doping. A notable advantage of RFET technology is its ability to achieve compact circuit topologies by utilizing fewer devices for various logic gates [8-14]. Typically, reconfigurable field effect transistors are controlled by two independent gate electrodes, with the program gate selecting the charge carrier type and the control gate regulating channel conductance and current. To attain identical transfer characteristics for both p-type and n-type operations, it is necessary to have a near mid-gap Schottky barrier height for both electrons and holes. The employment of $NiSi_2$ as the Schottky contact in Silicon based RFET devices has been experimentally proposed to provide an identical profile for both types of operation. Various configurations of RFET devices have been suggested for the development of reprogrammable logic devices. The triple gate RFET device, for instance, yields two threshold voltage values, thereby enabling the creation of two-stage logic circuits [15]. Meanwhile, the dehancement RFET device operates by utilizing two upper gates situated in the top and bottom layers of the channel. The program gate located in the lower region depletes the channel of its carriers, while the upper control gate regulates the device's on-state and off-state modes [16]. Furthermore, RFET devices based on emerging 2D materials may pave the way for more efficient logic circuit designs [17-19].

However, the conventional RFET device is subjected to a significant drawback, namely the low on-state current that arises from the constrained tunneling junction situated at the interface of the source and channel region. This paper presents a comprehensive assessment of the electrical characteristics of a novel RFET device that utilizes germanium as the channel material and features an extended source region. The proposed device boasts a wider source region that provides a greater tunneling area at the interface of the source and channel region, ultimately leading to improved drain current compared to conventional RFETs. To optimize device performance, critical design parameters are thoroughly investigated. The low carrier effective mass of germanium, in contrast to silicon, enhances the tunneling rate and may significantly improve the device's electrical performance.

The present paper is structured in the following manner: section two provides a comprehensive exploration of the device structure and the related simulation models. Subsequently, a thorough assessment is conducted on the impact of crucial structural and physical design parameters on the device's performance. Finally, the paper is outlined in the conclusion section.

2 Device Structure and Simulation Models

Figure 1a depicts the 2D schematics of a double gate extended source reconfigurable field effect transistor (ESRFET) utilizing germanium as the channel material. The appropriate bias for the electrodes to establish n-type and p-type operation can be found in Figs. 1b and 1c, respectively. Figure 1d presents the schematics of a conventional double gate RFET for comparison. Table 1 introduces the initial design parameters. The RFET device under consideration are comprised of two distinct gates, namely the control gate and the program gate. The control gate located in close proximity to the extended source region is accountable for both the operational on and off states of the device as well as the modulation of the tunneling barrier at the Schottky contact. In contrast, the program gate is responsible for regulating the band bending and determining the type of carrier that flows, whether it be in the p-FET or n-FET mode. The channel material of choice is germanium, a low-band channel material that successfully addresses the primary challenges of RFET development, namely lowering the threshold voltage and increasing the drive currents. Essentially, lowering the bandgap results in a decrease in the combined sum of p- and n-type Schottky barriers, thereby alleviating both challenges. The work function of the metal source and drain has been fine-tuned to a value of 4.34eV in order to achieve a Schottky barrier height of 0.34eV for electrons and a Schottky barrier height of 0.43eV for holes. This has resulted in nearly symmetrical transfer characteristics for both n-mode and p-mode operation. Numerical computations are carried out via Silvaco device simulator [20] and the following models are activated for accurately assessing the device performance:

(1) Thermionic emission model; The thermionic emission model serves as a critical carrier transport mechanism in ESRFET. This model pertains to the

release of thermally excited charge carriers from a metal surface. The outcome of thermionic emission is the production of a thermionic emission current, with carriers that possess energy above the Schottky barrier height able to pass over the barrier. Such an effect is more noticeable under conditions of elevated temperature and low Schottky barrier heights.

(2) Direct tunneling of carriers; basically, at elevated gate voltage values, the tunneling current has been observed to surpass the thermionic emission current, primarily owing to the reduction in the tunneling barrier width at the metal-semiconductor interface. The vertical and horizontal tunneling directions at the interface of the extended source and channel region are illustrated in Fig. 1a.

(3) Drift and diffusion models; in principle, carriers utilize thermionic emission and direct tunneling at the Schottky junction-interface and channel region. Nevertheless, the channel region experiences both drift and diffusion current until carriers reach the drain electrode. The drift current arises from the carriers' motion in reaction to an applied electric field, whereas the diffusion current arises from the migration of charge carriers from high to low concentration.;

(4) Auger and Shockley-read-hall (SRH) recombination models; the recombination models have been established to elucidate the influence of recombination and the production of carriers in the presence of defects and traps on the transport of carriers.

(5) Mobility models; the fundamental role of carrier drift velocity is significantly influenced by carrier mobility. The simulation takes into account the influence of horizontal and vertical electric fields on carrier mobility, and related models are employed. Additionally, the presence of dopants as impurities has an adverse impact on carrier mobility, leading to a reduction in velocity due to the scattering. Mobility models that account for the effect of dopants are also incorporated.

(6) Schottky barrier lowering model; The model of Schottky barrier lowering involves the buildup of image charges within the metal electrode of a metal-semiconductor junction. This phenomenon occurs as carriers come closer to the metal-semiconductor interface. The resulting potential created by this buildup decreases the effective barrier height, which can have a significant impact on device performance. Therefore, it is necessary to consider this effect in simulations.

(7) Quantum confinement model; the quantum confinement model is predominantly evident in thin channel thicknesses and produces energy sub-bands with heightened energy levels within the channel. This phenomenon results in an increase of the effective Schottky barrier height, which is fundamental to the simulation.

Table.1: Initial design parameters of ESRFET and conventional RFET

Parameter	ESRFET	Conventional RFET
Channel length -L_{ch}	43 nm	43nm
Spacer length	17 nm	17nm
Channel thickness-T_{ch}	10 nm	10nm
Control gate/ Program gate workfunction (WFG)	4.36 eV	4.36 eV
Program gate length	12nm	12nm
Control gate length	12nm	12nm
Channel doping density	intrinsic	intrinsic
Extended source length- L_S	10nm	-
Extended source thickness-T_S	5nm	-
Gate Oxide Thickness (HfO_2)	1nm	1nm

A concise summary of the fabrication process for the device is as follows: firstly, a layer of metal is applied onto a silicon wafer that has undergone oxidation. Subsequently, a process of dry etching is employed to create a bottom control gate and program gate electrode. Secondly, SiO_2 is deposited to serve as a spacer, and dry etching of the SiO_2 in the area of the bottom gate electrodes (control and program) is executed. Thirdly, HfO_2, the gate dielectric, is deposited and subjected to etching. Fourthly, Germanium is deposited through utilization of the low pressure chemical vapor deposition (LPCVD) technique. Fifthly, a thick layer of suitable metal (such as Ni) is applied onto the wafer by means of an electron beam evaporator, with the metal being selectively retained in the S/D region via a lift-off process. Sixthly, an annealing process is conducted to facilitate the formation of germanide. Seventhly, HfO_2

is deposited in order to establish the top gate electrode. Additionally, metal is deposited and etched to create the top control gate and program gate electrode. Lastly, SiO_2 is deposited to provide insulation between the gate electrode and the source and drain electrodes.

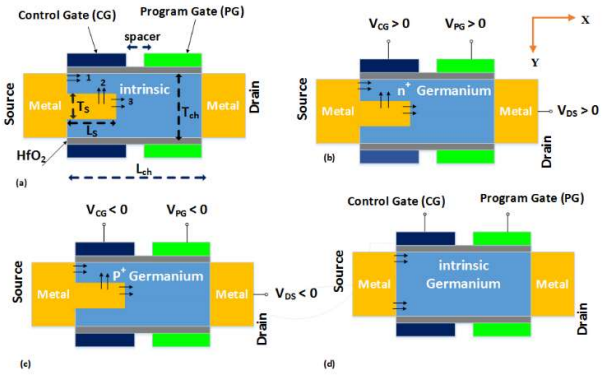

Figure 1. 2D schematic of (a) reconfigurable field effect transistor with extended source region. The tunneling directions at the interface of the source and channel regions in the vertical and horizontal directions are labeled as 1,2 and 3, (b) n-type operation of the RFET with extended source region, (c) p-type operation of the RFET with extended source region and (d) schematic of conventional RFET.

3 Results and Discussions

The operation principle of ESRFET is based on a gate modulated tunneling barrier at the interface of the Schottky contact and the channel region. Figure 2a and 2b illustrates the energy band diagram of the ESRFET in the off-state and on-state both in vertical and horizontal directions at the interface of the source and channel regions (directions are labeled as 1, 2, and 3 in Fig.1a), for p-type and n-type operation, respectively. It is observed that in the absence of control gate (i.e., V_{CG}=0, $V_{PG}\neq0$, $V_{DS}\neq0$), the tunneling barrier width is not thin enough for the carriers to tunnel through. In this situation, only limited carriers pass over the Schottky barrier via thermionic emission mechanism. However, as the control gate bias is elevated in the on state (i.e., $V_{CG}\neq0$, $V_{PG}\neq0$, $V_{DS}\neq0$) carriers are accumulated in the channel and the barrier width at the tunneling junction becomes narrow enough for direct tunneling of carriers. Unlike the conventional RFET with limited tunneling region, the main feature of the proposed ESRFET is the extended source region which provides a wide tunneling area. Evidently, the enhanced tunneling window increases the tunneling rate and improves the drain current.

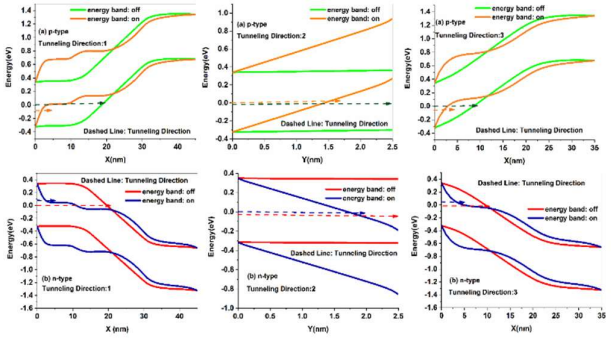

Figure 2. Energy band diagram of (a) p-type and (b) n-type device both in the off-state and on-state operation in vertical and horizontal tunneling directions, that are labeled as 1,2, and 3 in Fig 1a.

The hole density contour for operation of p-type and the related electron density for operation of n-type are depicted in the four panels of Fig. 3 in the off-state and on-state, respectively. It is evident that the density of transport carriers is considerably reduced at the source Schottky contacts and regions covered by the control gate in the absence of the control gate bias. However, once an appropriate bias with sufficient value is applied to the control gate in the on-state, carriers are accumulated in the channel and near the source Schottky contact to initiate tunneling.

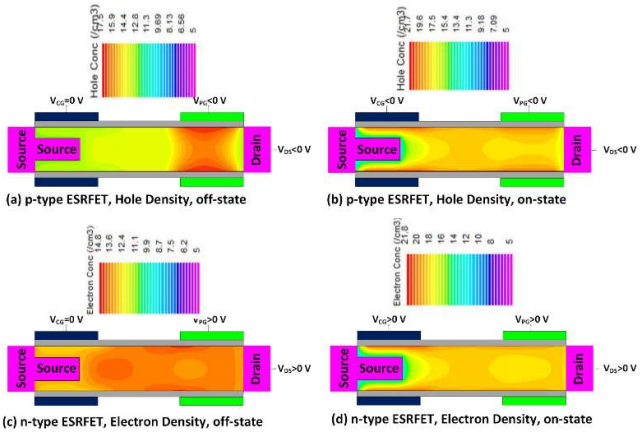

Figure 3. Carrier density of p-type and n-type ESRFET device in the off-state and on-state operation.

Figure 4 depicts the transfer characteristics of the ESRFET and the conventional RFET for comparison purposes. It is noticeable that the wider tunneling area of ESRFET produces a greater on-state current (I_{on}). Table 2 summarizes the electrical properties of the device. The threshold voltage (V_{th}) is defined as the control gate voltage required to achieve a drain current of 0.1 μA/μm. The outcomes indicate that the ESRFET has a lower threshold voltage and higher on-state current compared to the conventional RFET. On the contrary, owing to the expanded source area, the device

experiences a marginal rise in off-state current (I_{off}), which is attributed to the low band gap of germanium. Nevertheless, the thickness of the channel is adjusted such that the off-state current remains in the nano ampere range. In addition, the extended source length can be optimized to reduce the off-state current. By definition, subthreshold swing refers to the alteration in control gate voltage necessary to induce a tenfold (or an order of magnitude) change in the drain current.

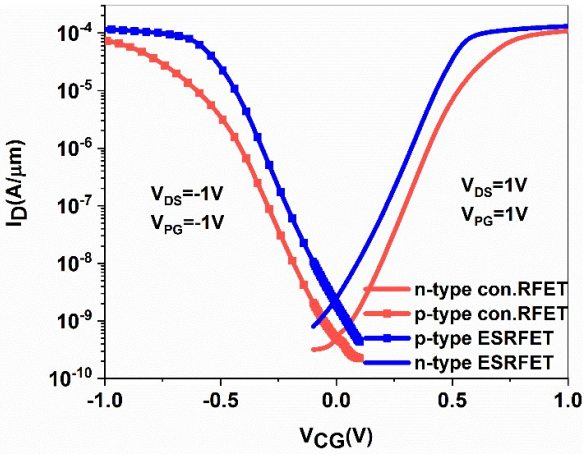

Figure 4. Transfer characteristics of ESRFET and conventional RFET in n-type and p-type operation.

Consequently, a lower subthreshold swing is preferable in order to achieve efficient high-speed switching. The findings establish that the extended source region in this paper leads to a lower subthreshold swing when compared to the conventional RFET. This in turn results in a higher switching speed for the extended source device.

Figure 5 depicts the transfer characteristics of the proposed ESRFET in both n-type and p-type modes of operation, as temperature is altered. The results clearly indicate that device performance diminishes with respect to off-state current and subthreshold swing as temperature increases. Thermionic emission, which is the thermally induced flow of charge carriers over a potential energy barrier, is defined as the root cause of this phenomenon. This is due to the fact that thermal energy provided to the carrier surpasses the work function of the metal source/drain electrodes, allowing carriers to overcome the Schottky barrier prior to the onset of tunneling, resulting in an increase in the off-state current and degradation of the subthreshold swing.

Table 2. Electrical characteristics of ESRFET and conventional RFET.

Electrical Measure	**I_{on} (A/μm)**		**I_{off} (A/μm)**	
Type of the Device	n-type	p-type	n-type	p-type
Conventional RFET	1.09×10^{-4}	7.42×10^{-5}	5.04×10^{-10}	5.04×10^{-10}
ESRFET	1.31×10^{-4}	1.16×10^{-4}	2.48×10^{-9}	1.97×10^{-9}
Electrical Measure	**V_{th} (V)**		**Ion/Ioff**	
Type of the Device	n-type	p-type	n-type	p-type
Conventional RFET	0.293	-0.296	2.16×10^{5}	1.47×10^{5}
ESRFET	0.212	-0.217	5.26×10^{4}	5.90×10^{4}
Electrical Measure	**Subthreshold Swing(mV/dec)**			
Type of the Device	n-type	p-type		
Conventional RFET	113	121		
ESRFET	106	110		

The work function of the gate (control gate and program gate) is a crucial factor in the design process, as it can impact the distribution of charges within the channel. As demonstrated in Fig. 6, the transfer characteristics of the ESRFET for both n-type and p-type modes of operation are affected by the gate work function. In the case of n-type mode, the drain current decreases with an increase in the work function of the control and program gates, due to the reduction of electron density in the channel. Conversely, for p-type

operation, an opposite trend is observed in the drain current, resulting from the accumulation of holes at the tunneling junction.

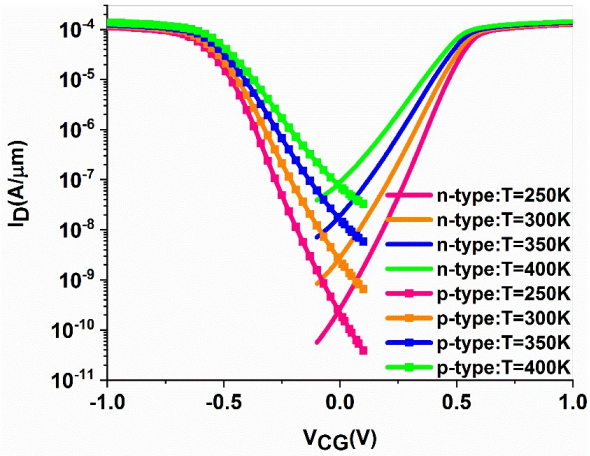

Figure 5. Transfer characteristics of ESRFET for n-type and p-type operation as the temperature is varied.

Nevertheless, when the gate work function surpasses 4.5eV, the off-state current for n-type experiences a considerable increase, leading to an enhanced threshold voltage. This outcome is attributed to the accumulation of excessive holes in the channel, which increases the gate-induced drain leakage (GIDL) current mechanism. Determining the most favorable work function for the gate materials with the objective of achieving the minimum off-state current for both n-type and p-type operation is of utmost importance.

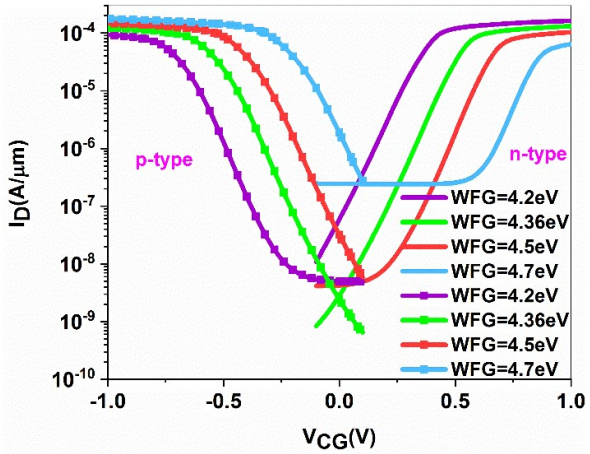

Figure 6. I_D-V_{CG} curves of ESRFET for n-type and p-type as the work function of the control gate and program gate are parametrized.

The panels of Fig. 7, depict the influence of the extended source length on the transfer characteristics of the device for both n-type and p-type operations, respectively. It has been noted that an increase in the source extended length results in an increase in the on-state current and a lower threshold voltage can be achieved. This effect is primarily ascribed to the broader tunneling area at the interface of the source and channel. Nevertheless, when the source extended length surpasses 14nm, which is equivalent to the length of the control gate, the device performance deteriorates. Fundamentally, as the source region extends towards the program gate region, the device loses the control gate's controllability over the channel, and the tunneling is no longer reliant on the electric field of the control gate. The results demonstrate that L_S=8nm is the optimum length with low off-state current and improved on-state current.

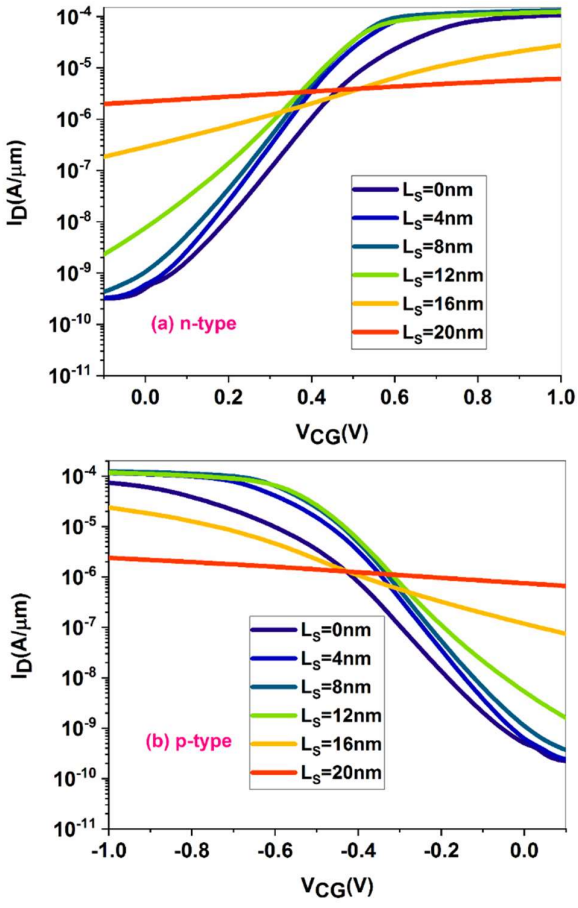

Figure 7. Transfer characteristics of ESRFET as the extended source length is varied for (a) n-type, and (b) p-type operation.

Figure 8 shows the output characteristic of the suggested ESRFET, as the control gate bias is modified, for both n-type and p-type operations in logarithmic scales. The findings reveal that a substantial enhancement in the drain current is observed when the control gate bias surpasses the prescribed voltage for the onset of tunneling. Furthermore, a significant correlation between the channel conductance and the variation in control gate bias is discovered. It is apparent that through an increase in the control gate bias, a sufficient number of carriers are accumulated, leading to the formation of a channel with low resistance between the source and drain.

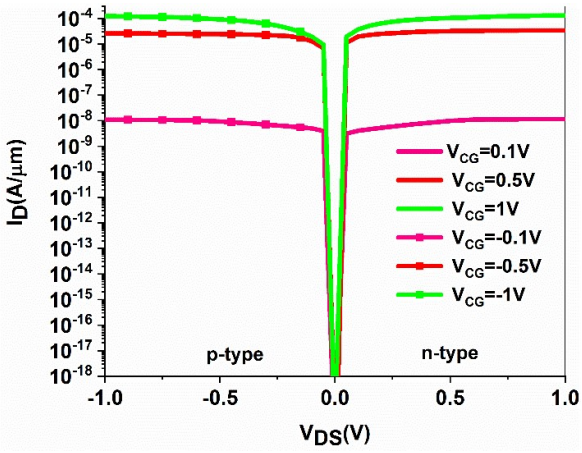

Figure 8. Output characteristics of ESRFET for n-type and p-type operation, as the control gate bias is varied.

The effect of channel thickness on the performance of ESRFET is depicted in Fig. 9, for n-type and p-type operation. The thickness of the extended source region is considered constant at Ts=5nm. It is observed that as the channel thickness increases, the device performance degrades in terms of on-state current and subthreshold swing. Basically, this effect is mainly attributed to the degradation of the controllability of the gate over the channel potential for thicker channel thicknesses. Essentially, enhancing the on-state current of a device can be achieved by increasing the width of the extended source region or, in simpler terms, by decreasing the gap between the source region and the control gate. Nonetheless, it is imperative to note that determining the optimal thickness for the extended source region is crucial. It is evident that as the thickness of the extended source region enhances, the thickness of the channel located above or below it decreases, thereby increasing the controllability of the gate over the channel and resulting in a higher on-state current. However, excessive increment of the extended source thickness leads to the depletion of the channel layer due to the Schottky contact space charge region, resulting in an increase in the device threshold voltage. The frequency response of ESRFET is demonstrated in Fig. 10. The outcomes reveal that cut-off frequency f_T=3GHz is achieved for n-type and p-type devices, which manifests the feasibility of the device for high frequency applications.

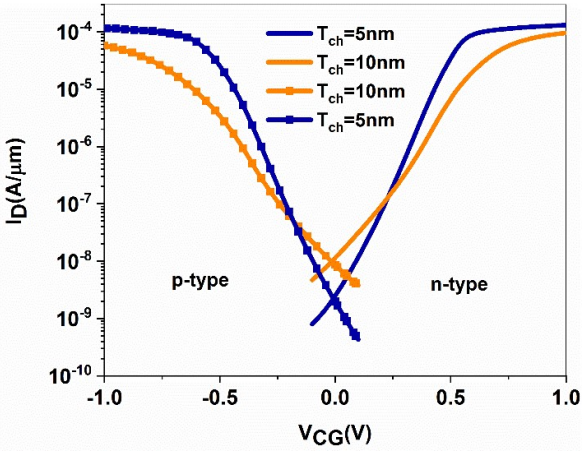

Figure 9. Transfer characteristics of ESRFET for n-type and p-type operation as the channel thickness is varied.

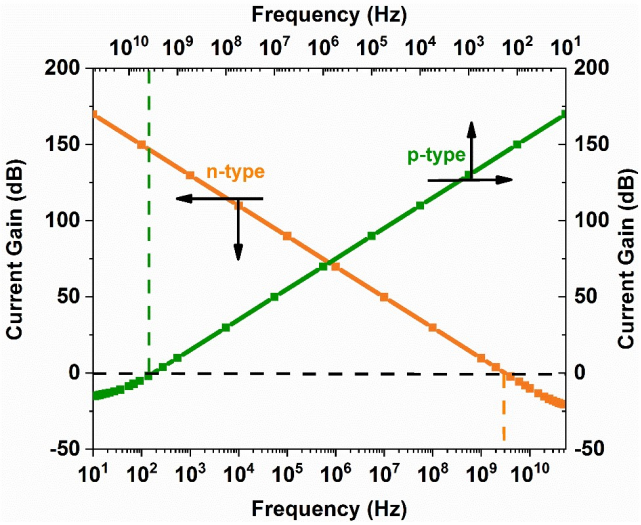

Figure 10. Current gain versus frequency of ESRFET for n-type and p-type operation.

Table.3. the electrical parameters of RFET devices are compared with the proposed extended source device.

Ref.	Experimental/ Simulation	Channel Length	Channel Material
[11]	Simulation	26nm	Silicon
[13]	Simulation	90nm	Silicon
[14]	experimental	630nm	Silicon
[15]	Simulation	24nm	Silicon
This work	Simulation	43nm	Germanium
Ref.	On-sate current		Bias value
	n-type	p-type	
[11]	0.549×10^{-6} (A)	1.39×10^{-6} (A)	$V_{CG}=\pm1V$ $V_{PG}=\pm1V$
[13]	3×10^{-4} (A/μm)	1×10^{-4} (A/μm)	$V_{CG}=\pm1.5V$ $V_{PG}=\pm1.5V$
[14]	1×10^{-7} (A)	1×10^{-6} (A)	$V_{CG}=\pm3V$ $V_{PG}=\pm3V$
[15]	35 (μA)	30 (μA)	$V_{CG}=\pm1.2V$ $V_{PG}=\pm1.2V$
This work	1.31×10^{-4} (A/μm)	1.16×10^{-4} (A/μm)	$V_{CG}=\pm1V$ $V_{PG}=\pm1V$

4 Conclusions

In this paper, a comprehensive investigation into the electrical characteristics of a Schottky barrier reconfigurable transistor with an extended source region has been conducted. The impact of critical design parameters on the device's performance has been meticulously evaluated. The findings reveal that the on-state current is significantly enhanced by the presence of the extended source region, which provides a wider tunneling area. It is imperative to note that the optimal length of the extended source should be equal to that of the control gate; otherwise, the control gate's controllability over the channel will be compromised, and the electrical performance of the device will deteriorate. The gate work function is a crucial design parameter that must be determined to ensure the lowest possible off-state current is achieved for both n-type and p-type operation. The optimal values of critical design parameters, namely the channel thickness and the extended source thickness, are crucial in achieving the lowest possible voltage for the onset of tunneling and improved electrical performance. It is imperative to carefully optimize the extended source thickness, as a thicker extended source region can lead to depletion of the channel region due to the space charge region of the Schottky contact, thereby increasing the required voltage for the onset of tunneling. Conversely, a thinner extended source region can negatively impact the subthreshold swing and reduce the gate controllability over the channel region. The proposed ESRFET offers a high cut-off frequency, which makes it suitable for low power high frequency applications.

4 References

[1] Aishwarya Kaity, Sangeeta Singh, P. N. Kondekar. "Silicon-on-nothing electrostatically doped junction less tunnel field effect transistor (SON-ED-JLTFET): A short channel effect resilient design." Silicon, **13** (2021) 9-23.

[2] Nassima Bourahla, Ahmed Bourahla, Baghdad Hadri. "Comparative performance of the ultra-short channel technology for the DG-FinFET characteristics using different high-k dielectric materials." Indian Journal of Physics, **95** (2021) 1977-1984.

[3] Kerim Yılmaz, Ghader Darbandy, Gilles Reimbold, Benjamin Iniguez, Francois Lime, Alexander Kloes. "Equivalent DG dimensions concept for compact modeling of short-channel and thin body GAA MOSFETs including quantum confinement." IEEE Transactions on Electron Devices, **67** (2020) 5381-5387.

[4] Mile Schwarz, Laurie E. Calvet, John P. Snyder, Tillmann Krauss, Udo Schwalke, Alexander Kloes. "On the physical behavior of cryogenic IV and III–V Schottky barrier MOSFET devices." IEEE Transactions on

Electron Devices, **64** (2017) 3808-3815.

[5] Prashanth Kumar, WasimArif, Brinda Bhowmick. "Scaling of dopant segregation Schottky barrier using metal strip buried oxide MOSFET and its comparison with conventional device." Silicon, **10** (2018) 811-820.

[6] Prashanth Kumar Brinda Bhowmick. "Source-drain junction engineering Schottky barrier MOSFETs and their mixed mode application." Silicon, **12** (2020) 821-830.

[7] Amit Saxena, Manoj Kumar, R. K. Sharma, and R. S. Gupta. "SOI Schottky barrier nanowire MOSFET with reduced ambipolarity and enhanced electrostatic integrity." Journal of Electronic Materials **49** (2020) 4450-4456.

[8] Bin Sun, Benjamin Richstein, Patrick Liebisch, Thorben Frahm, Stefan Scholz, Jens Trommer, Thomas Mikolajick, and Joachim Knoch. "On the operation modes of dual-gate reconfigurable nanowire transistors." IEEE Transactions on Electron Devices, **68** (2021) 3684-3689.

[9] Christian Roemer, Ghader Darbandy, Mike Schwarz, Jens Trommer, André Heinzig, Thomas Mikolajick, Walter M. Weber, Benjamín Iñíguez, Alexander Kloes. "Physics-based dc compact modeling of schottky barrier and reconfigurable field-effect transistors." IEEE Journal of the Electron Devices Society, **10** (2021) 416-423.

[10] C. Navarro, S. Barraud, S. Martinie, J. Lacord, M. A. Jaud, M. Vinet. "Reconfigurable field effect transistor for advanced CMOS: Advantages and limitations." Solid-State Electronics, **128** (2017) 155-162.

[11] Yan Yao, Yabin Sun, Xiaojin Li, Yanling Shi, Ziyu Liu. "Novel reconfigurable field-effect transistor with asymmetric spacer engineering at drain side." IEEE Transactions on Electron Devices, **67** (2020) 751-757.

[12] Jong-Ho Bae, Hyeongsu Kim, Dongseok Kwon, Suhwan Lim, Sung-Tae Lee, Byung-Gook Park, Jong-Ho Lee. "Reconfigurable field-effect transistor as a synaptic device for XNOR binary neural network." IEEE Electron Device Letters, **40** (2019) 624-627.

[13] Daehoon Wee, Hui Tae Kwon, Won Joo Lee, Hyun-Seok Choi, Yu Jeong Park, Boram Kim, Yoon Kim. "U-shaped Reconfigurable Field-effect Transistor." Journal of Semiconductor Technology and Science **19** (2019): 63-68.

[14] André Heinzig, Stefan Slesazeck, Franz Kreupl, Thomas Mikolajick, Walter M. Weber. "Reconfigurable silicon nanowire transistors." Nano letters, **12** (2012) 119-124.

[15] Jian Zhang, Pierre-Emmanuel Gaillardon, Giovanni De Micheli. "Dual-threshold-voltage configurable circuits with three-independent-gate silicon nanowire FETs." In 2013 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 2111-2114. IEEE, 2013.

[16] Tillmann Adrian Krauss, Frank Wessely, Udo Schwalke. "Favorable combination of Schottky barrier and junctionless properties in field-effect transistors for high temperature applications." ECS Transactions, **75** (2016) 57.

[17] Wenwen Fei, Jens Trommer, Max Christian Lemme, Thomas Mikolajick, André Heinzig. "Emerging reconfigurable electronic devices based on two-dimensional materials: A review." InfoMat, **4** (2022) e12355.

[18] Yue Zhou, Yasai Wang, Fuwei Zhuge,

Jianmiao Guo, Sijie Ma, Jingli Wang, Zijian Tang et al., "A Reconfigurable Two-WSe2-Transistor Synaptic Cell for Reinforcement Learning." Advanced Materials, **34** (2022) 2107754.

[19] Yoshitaka Shingaya, Amir Zulkefli, Takuya Iwasaki, Ryoma Hayakawa, Shu Nakaharai, Kenji Watanabe, Takashi Taniguchi, Yutaka Wakayama. "Dual-Gate Anti-Ambipolar Transistor with Van der Waals ReS2/WSe2 Heterojunction for Reconfigurable Logic Operations." Advanced Electronic Materials **9** (2023) 2200704.

[20] ATLAS User Manual, Santa Clara, USA: Silvaco International, (2015).